IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Benjamin M. Rice
Serial No.:	10/830,171
Filing Date:	April 23, 2004
Group Art Unit:	2838
Examiner:	Adolf Berhane
Title:	SWITCH CONTROLLER FOR A POWER CONTROL SYSTEM AND METHOD THEREFOR

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO:
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Semiconductor Components Industries, LLC
Name of Assignee
Lydia McNamara 9/19/04
SIGNATURE DATE

AFFIDAVIT UNDER 37 CFR 1.131

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SIR:

I, Benjamin M. Rice, 141 Pleasant Street #9, Attleboro, Massachusetts, 02703, being duly sworn, depose and say that I am the applicant of the above-identified patent application.

Deponent states that claims 1-3 and 5-20 (hereinafter "Claims") were rejected under 35 USC 102, based on a United States Patent No. 7,002,325 B2 of Matthew B. Harris et. al. (hereinafter "Art"); that I have examined a copy

of the Art which only has an effective United States filing date that relates back to a provisional filing date of October 20, 2003 (hereinafter "Date") and a publication date of April 21, 2005; and that the Art does not claim the rejected inventions.

Deponent states that prior to the Date, I completed, in the United States, the above-referenced inventions as more fully pointed out hereinafter by recital of facts showing conception prior to the Date, coupled with due diligence from prior to said Date to subsequent reduction to practice or filing of the above-identified patent application; and that I made and completed the above-identified inventions while employed by Semiconductor Components Industries, L.L.C (hereinafter "ON Semi") having its principal office in Phoenix, Arizona, assignee of the invention.

Deponent further states that:

1. Attached hereto is a true copy of an engineering drawing of Deponent showing an interconnect configuration and notes illustrating a method of controlling a switch controller which is disclosed by and is in accordance with the above-identified application; and that even though this page does not carry a date, the page was made during an ON Semi meeting conducted at the Crown Plaza resort at a date prior to the Date;

2. Deponent diligently made a detailed drawing of the configuration, a true copy of which is attached hereto; and that the detailed drawing was made as a computer file prior to the Date as shown by the attached filename listing that shows a modification date of the file, which has been blocked off, prior to the Date;

3. Deponent diligently made a detailed flowchart, a true copy of which is attached hereto, more formally illustrating the method of controlling a switch controller in accordance with the detailed drawing and in accordance

with the above-identified application; and that the detailed flowchart was made as a computer file prior to the Date as shown by the attached filename listing that shows a modification date of the file, which has been blocked off, prior to the Date;

4. Deponent diligently made a detailed state diagram, a true copy of which is attached hereto, illustrating different states of the method of controlling a switch controller in accordance with flowchart, the detailed diagram, and in accordance with the above-identified application; that the detailed state diagram bears a date,which has been blocked off, prior to the Date; and that the detailed state diagram was made as a computer file prior to the Date as shown by the attached filename listing that shows a modification date of the file, which has been blocked off, prior to the Date;

5. Deponent diligently reduced to practice the inventions of the above referenced application as shown by a detailed Spice simulation file, a true copy of which is attached hereto; Deponent ran simulations thereof as an actual reduction to practice, the Spice simulation file and simulation thereof being in accordance with the above-identified application; and that the Spice simulation file bears a date, which has been blocked off, prior to the Date;

6. Deponent diligently disclosed the above-identified inventions to the ON Semi Patent department as shown by a hereto attached true copy of a disclosure input and recording form having a date of December 9, 2003;

7. The disclosure input and recording form was reviewed by the ON Semi patent management committee, and a patent application was prepared disclosing and claiming inventions in the disclosure input and recording form; the application was reviewed by Deponent which led to filing of the above-referenced application on April 23, 2004.

Deponent further states that I do not know and do not believe that the invention has been in public use or on sale in this country, or patented or described in a printed publication in this or any foreign country for more than one year prior to the application's filing date and I have never abandoned the invention.

Deponent respectfully prays that the Claims which define his invention, be allowed.

Benjamin M. Rice

Benjamin M. Rice

STATE OF Rhode Island)
:
COUNTY OF KENT)

I, JUDITH A KEENAN, a Notary Public in and for the County and State aforesaid, do hereby certify that

BENJAMIN M. RICE

whose name(s) is (are) subscribed to the foregoing instrument, appeared before me this day in person and acknowledged that he/she/they signed, sealed, and delivered the said instrument as his/her/their free and voluntary act and deed for the uses and purposes therein set forth.

Given under my hand and notarial seal this 14 day of September, 2006.

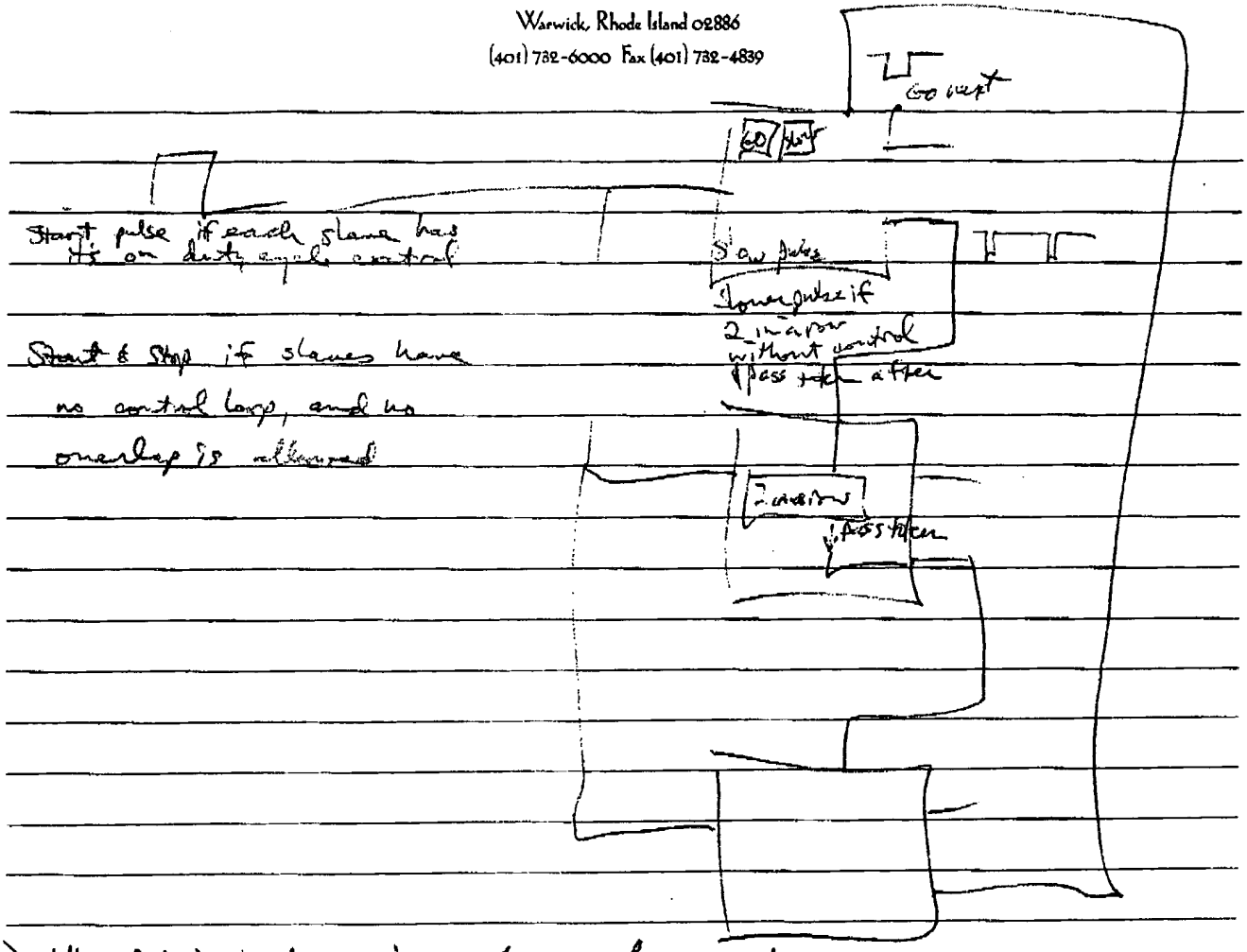
Judith A Keenan
Notary Public
My Commission Expires:
6-27-09

Seal

1 Extra Pin Token method

CROWNE PLAZA®
HOTELS · RESORTS

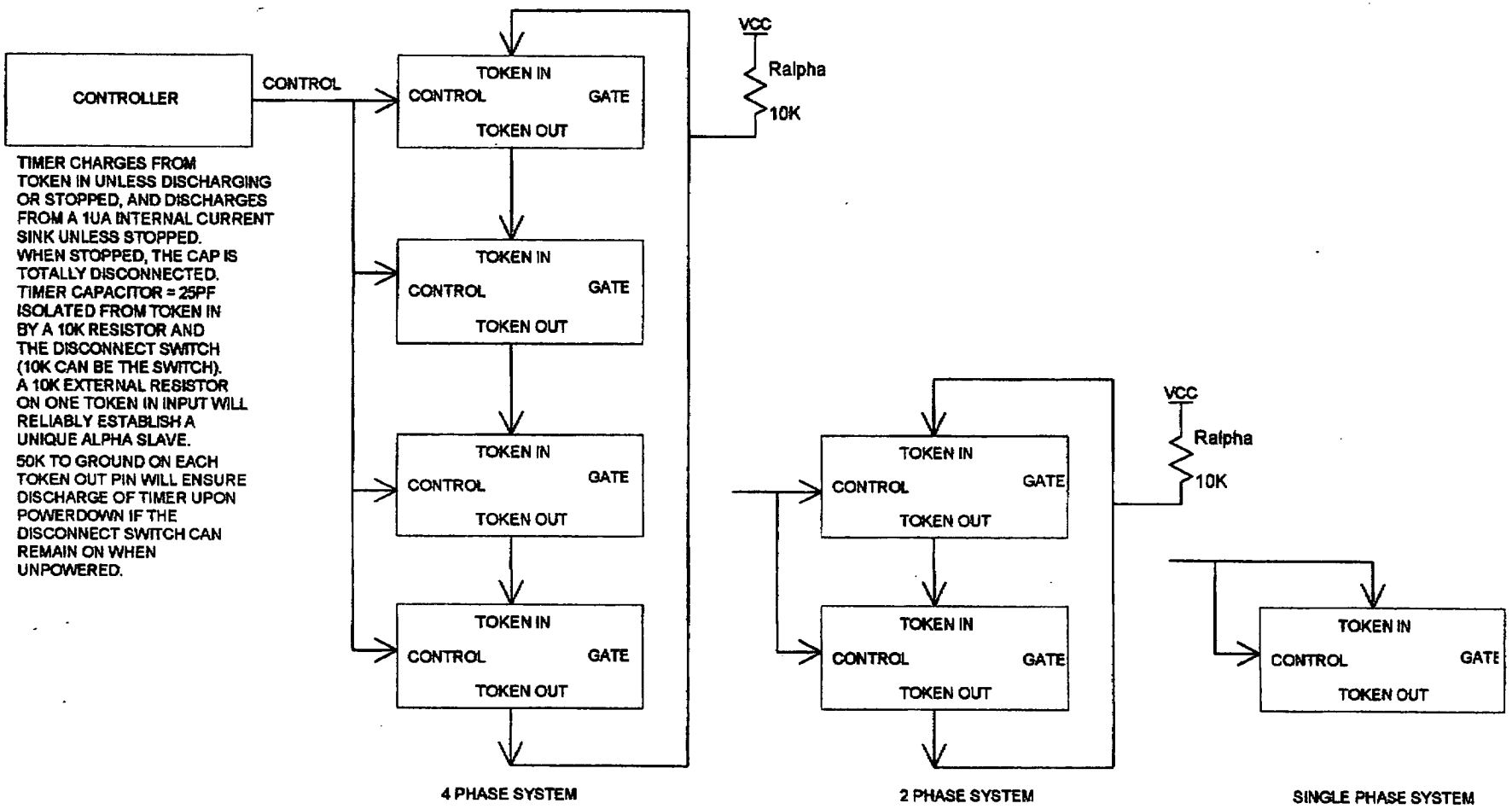
801 Greenwich Avenue
Warwick, Rhode Island 02886
(401) 732-6000 Fax (401) 732-4839

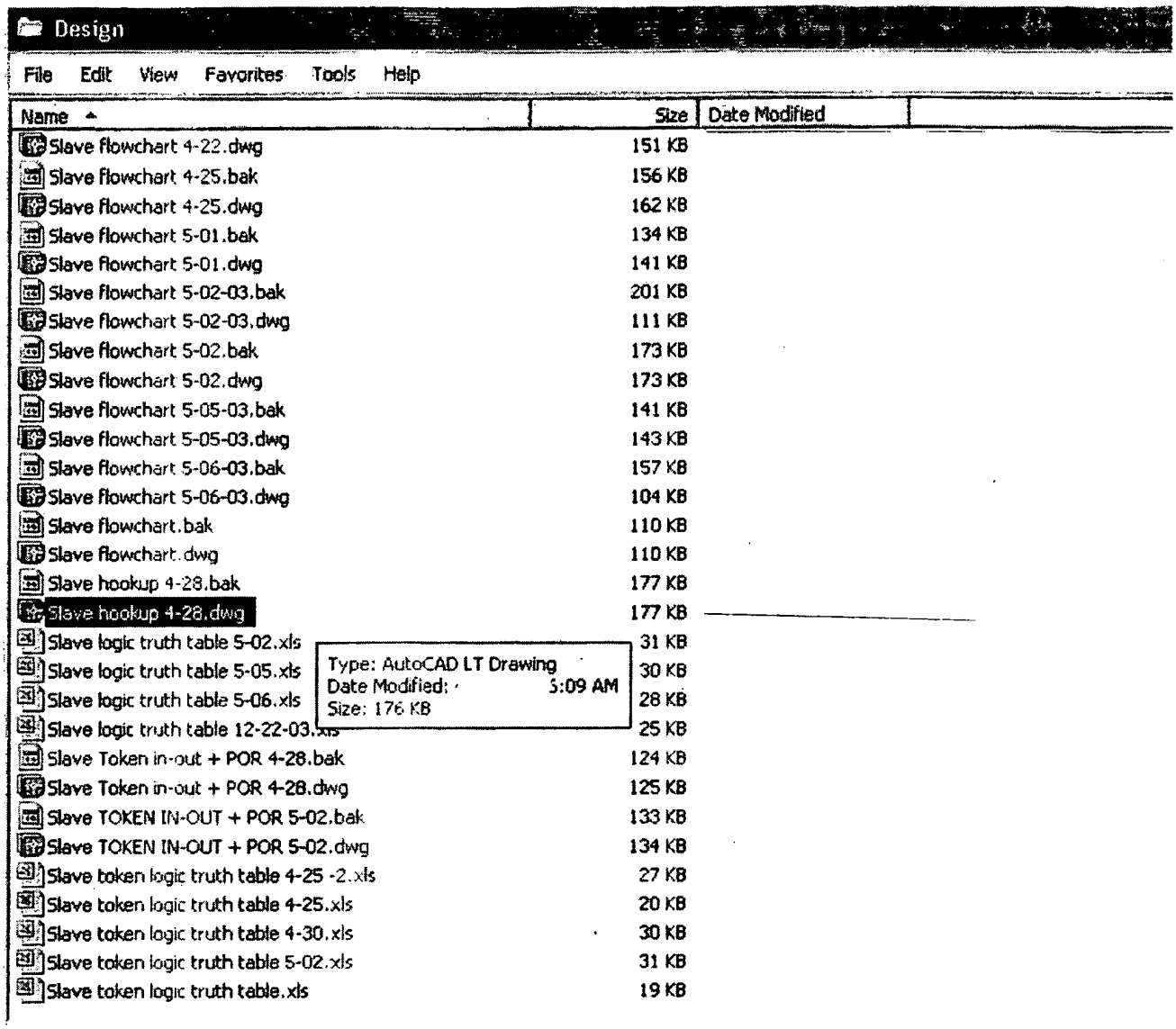


1) All units start timer when they wake
2) set "#1" latch

2) If timer times out before getting a token, send a token, then retire.
If receive a token before timeout - immediately pass it on, and reset "#1" latch. Continue to pass all tokens received. (Set longer timer?)

3) When control pulse received, 1) initiate phase if "#1" latch set.
2) Stop ~~passing~~ tokens - use tokens per normal.


CONTROLLER
CONTROL
TOKEN IN
CONTROL
GATE
TOKEN OUT
VCC
Ralpha
10K
TIMER CHARGES FROM TOKEN IN UNLESS DISCHARGING OR STOPPED, AND DISCHARGES FROM A 1UA INTERNAL CURRENT SINK UNLESS STOPPED. WHEN STOPPED, THE CAP IS TOTALLY DISCONNECTED. TIMER CAPACITOR = 25PF ISOLATED FROM TOKEN IN BY A 10K RESISTOR AND THE DISCONNECT SWITCH (10K CAN BE THE SWITCH). A 10K EXTERNAL RESISTOR ON ONE TOKEN IN INPUT WILL RELIABLY ESTABLISH A UNIQUE ALPHA SLAVE.
50K TO GROUND ON EACH TOKEN OUT PIN WILL ENSURE DISCHARGE OF TIMER UPON POWERDOWN IF THE DISCONNECT SWITCH CAN REMAIN ON WHEN UNPOWERED.
4 PHASE SYSTEM
2 PHASE SYSTEM
SINGLE PHASE SYSTEM
FOR SINGLE PHASE SYSTEM OR GANGED PHASES, TIE TOKEN IN TO CONTROL IN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Name
Size
Date Modified
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Slave flowchart 4-25.bak 156 KB
Slave flowchart 4-25.dwg 162 KB
Slave flowchart 5-01.bak 134 KB
Slave flowchart 5-01.dwg 141 KB
Slave flowchart 5-02-03.bak 201 KB
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Slave logic truth table 5-05.xls 30 KB
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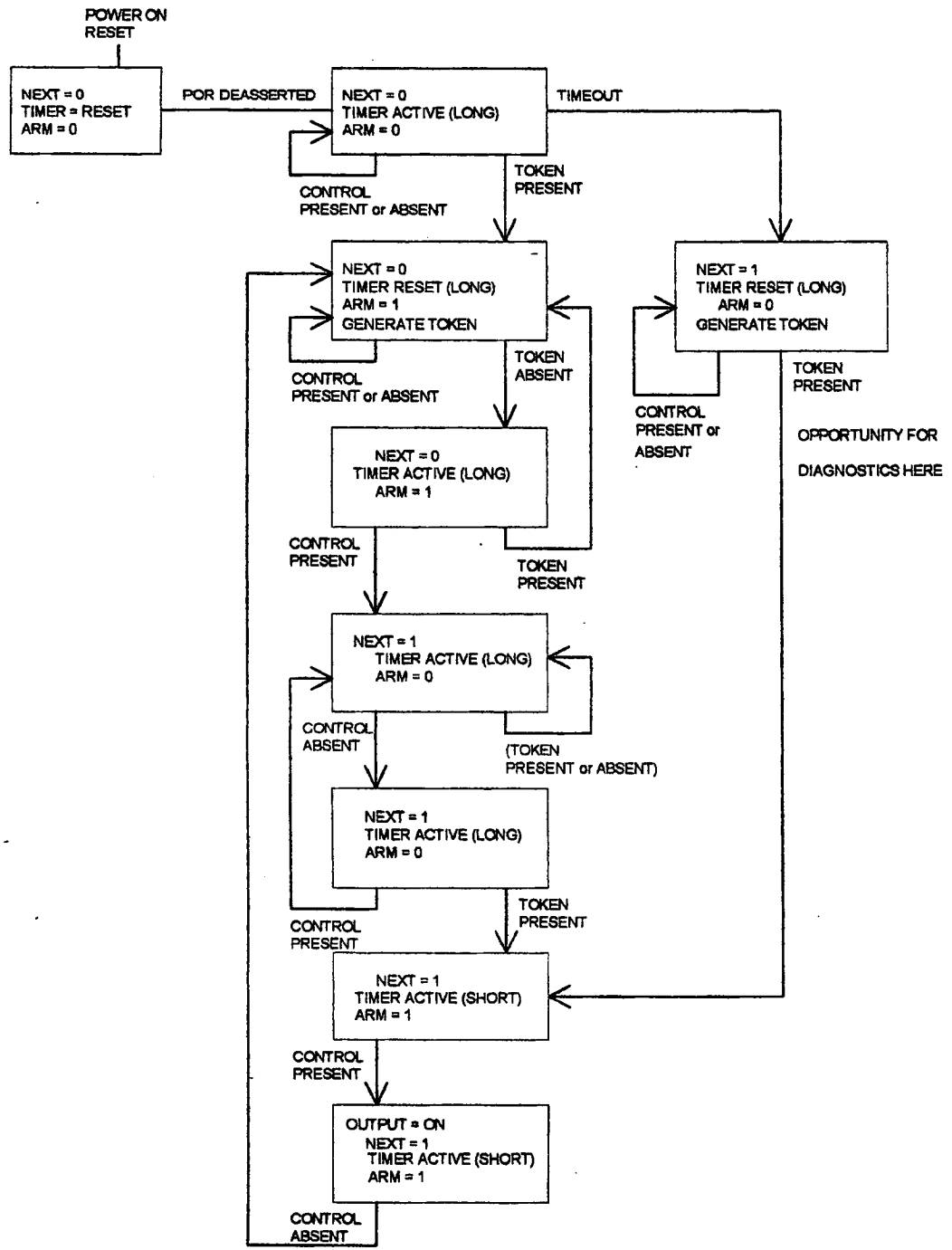
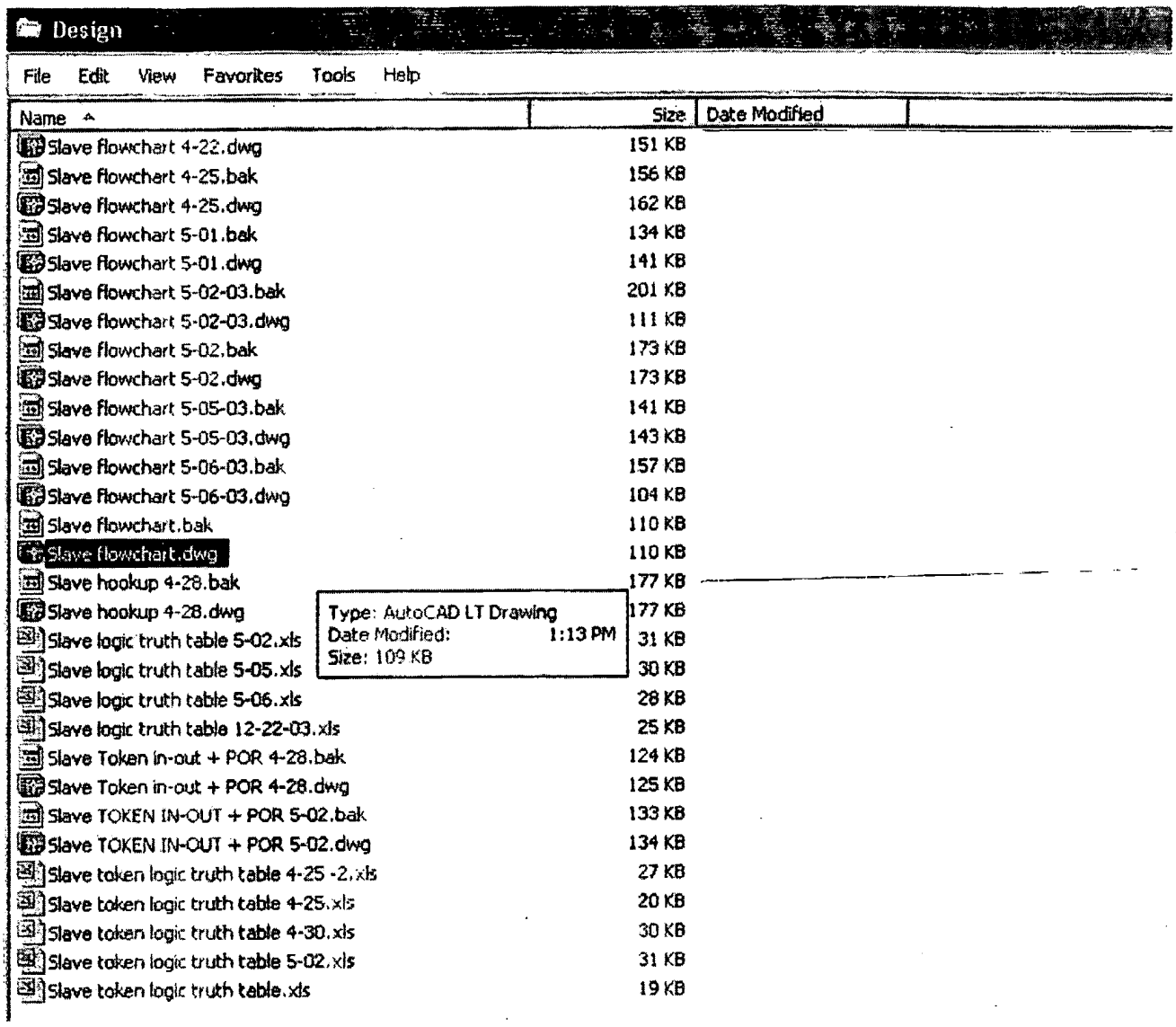

POWER ON
RESET
NEXT = 0
TIMER = RESET
ARM = 0
POR DEASSERTED
NEXT = 0
TIMER ACTIVE (LONG)
ARM = 0
TIMEOUT
CONTROL
PRESENT or ABSENT
TOKEN
PRESENT
NEXT = 0
TIMER RESET (LONG)
ARM = 1
GENERATE TOKEN
NEXT = 1
TIMER RESET (LONG)
ARM = 0
GENERATE TOKEN
CONTROL
PRESENT or ABSENT
TOKEN
ABSENT
TOKEN
PRESENT
CONTROL
PRESENT or
ABSENT
OPPORTUNITY FOR
DIAGNOSTICS HERE
NEXT = 0
TIMER ACTIVE (LONG)
ARM = 1
CONTROL
PRESENT
TOKEN
PRESENT
NEXT = 1
TIMER ACTIVE (LONG)
ARM = 0
CONTROL
ABSENT
(TOKEN
PRESENT or ABSENT)
NEXT = 1
TIMER ACTIVE (LONG)
ARM = 0
CONTROL
PRESENT
TOKEN
PRESENT
NEXT = 1
TIMER ACTIVE (SHORT)
ARM = 1
CONTROL
PRESENT
OUTPUT = ON
NEXT = 1
TIMER ACTIVE (SHORT)
ARM = 1
CONTROL
ABSENT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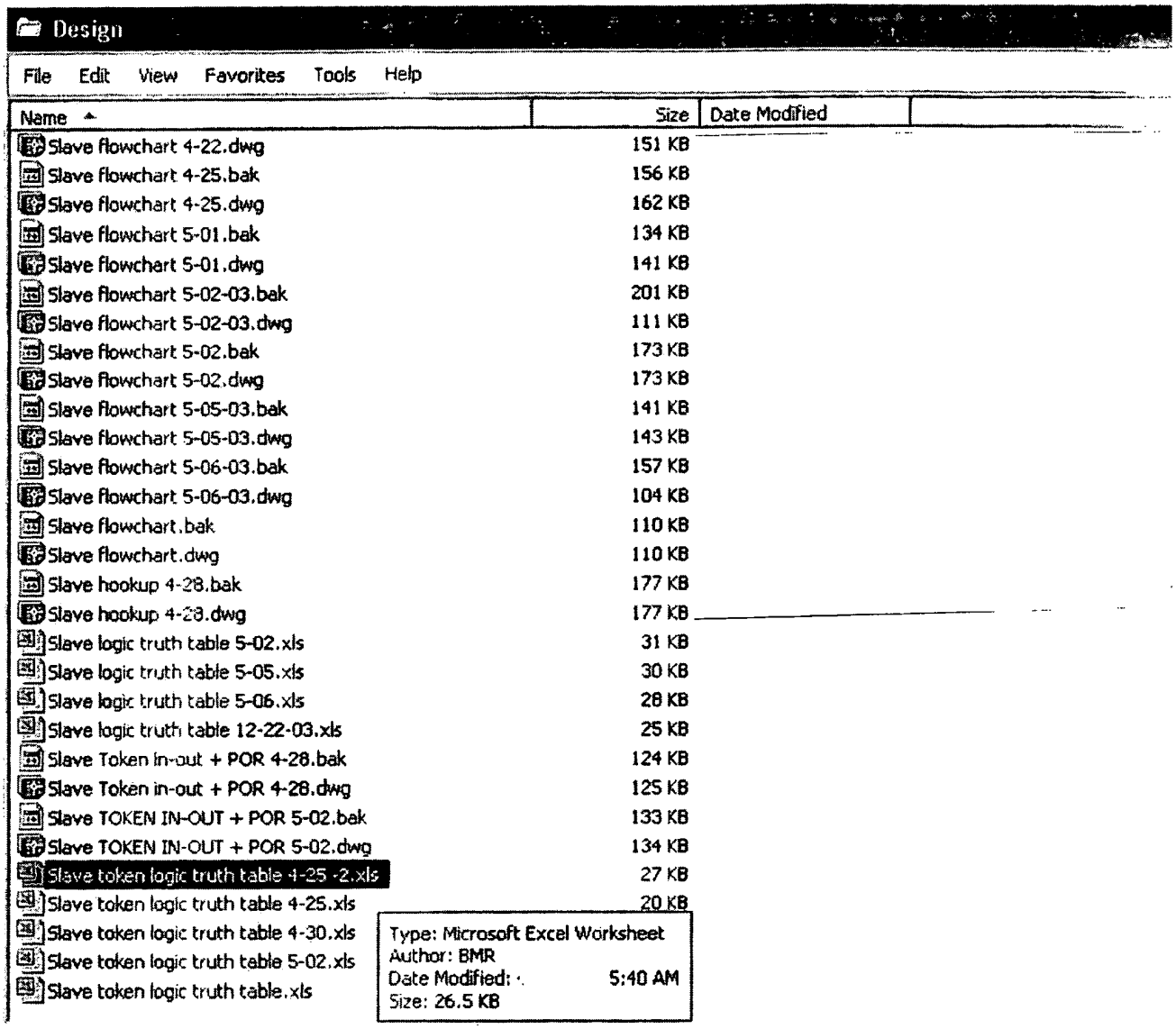
Slave token logic truth table ___ xls

	ENTERED			BOLD = CHANGE										
	FROM	INPUTS					OUTPUTS						GOES TO	
STATE	STATE	POR	NEXT	ARM	TOKIN	CONTROL	NEXT	ARM	TOKOUT	GATE	SWIN	SWOUT	STATE	
0		< 0.3V	X	X	X	X	0	0	0	0	ON	ON	1	Initial Power ON Reset
1	0	**>0.3V, <1.5V**	0	0	X	X	0	0	0	0	ON	ON	2 or 3	After POR, before Alpha Slave established
2	1	**> 1.5V**	0	0	0	X	0	1	**1**	0	ON	ON	4 (or 6)	Establishes first impending Alpha Slave
3	1	> 0.3V, < 1.5V	0	0	1	X	0	1	**1**	0	ON	ON	4	After POR, after Alpha Slave established
4	2,3,12,14	> 0.3V	0	1	1	X	0	1	1	0	ON	ON	5	Inactive Slave
5	4,13	> 0.3V	0	1	**0**	X	**1**	**0**	1	0	**OFF**	**OFF**	6	1st step of promotion to Alpha Slave
6	2,4	> 0.3V	1	0	0	X	1	0	1	0	OFF	OFF	7,8	Waiting for final step of promotion to Alpha Slave
7	6	> 0.3V	1	0	**1**	0	1	1	**0**	0	OFF	**ON**	10	Multi-phase promotion to Alpha Slave
10	7	> 0.3V	1	- 1	X	0	1	1	0	0	OFF	ON	11 or 14	Alpha waiting for control pulse (multi only)
11	10,8	> 1.5V	1	1	1	**1**	**0**	**0**	0	**1**	**ON**	ON	12	Alpha receives control pulse
12	11	> 1.5V	0	0	1	1	0	0	0	1	ON	ON	13	Alpha during control pulse
13	12	> 1.5V	0	0	X	**0**	0	**1**	**1**	**0**	ON	ON	4	Alpha end of control pulse
14	10	**< 1.5V**	1	1	X	0	**0**	1	**1**	0	**ON**	ON	4	Alpha gives up waiting for control pulse
FLOW						TOKEN OUT is POR>0.3 AND (NEXT XOR ARM)								
0						GATE is NOT TOKOUT AND NOT (NEXT XOR ARM)								
1	>>>	3				SWIN is OFF when NEXT = 1								
2		V				SWOFF is OFF when NEXT = 1, ARM = 0								
4	<<<	<<<	<<<	<<<										
5		^		^										
6		^		^										
7		^		^										
10		^		^										
11	>>>	14		^										
12				^										
13	>>>	>>>	>>>	>>>										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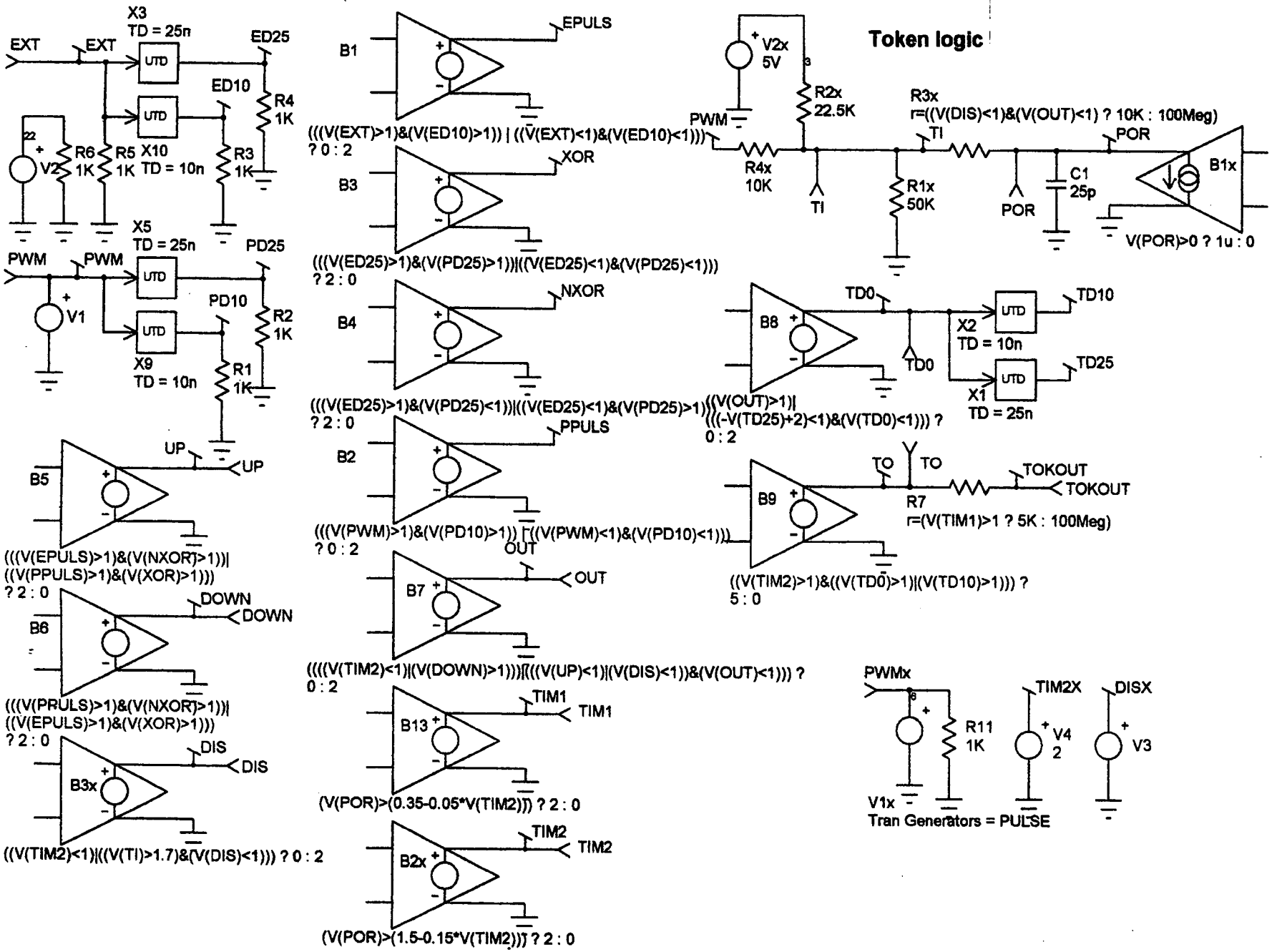
X3
TD = 25n
EXT
EXT
UTD
ED25
ED10
R4
1K
UTD
X10
TD = 10n
R6
1K
R5
1K
R3
1K
V2
X5
TD = 25n
PWM
PWM
UTD
PD25
PD10
R2
1K
V1
UTD
X9
TD = 10n
R1
1K
B1
EPULS
(((V(EXT)>1)&(V(ED10)>1)) | ((V(EXT)<1)&(V(ED10)<1))) ? 0 : 2
B3
XOR
(((V(ED25)>1)&(V(PD25)>1))|((V(ED25)<1)&(V(PD25)<1))) ? 2 : 0
B4
NXOR
(((V(ED25)>1)&(V(PD25)<1))|((V(ED25)<1)&(V(PD25)>1))) ? 2 : 0
B2
PPULS
(((V(PWM)>1)&(V(PD10)>1)) | ((V(PWM)<1)&(V(PD10)<1))) ? 0 : 2
B5
UP
UP
(((V(EPULS)>1)&(V(NXOR)>1))| ((V(PPULS)>1)&(V(XOR)>1))) ? 2 : 0
B6
DOWN
DOWN
(((V(PRULS)>1)&(V(NXOR)>1))| ((V(EPULS)>1)&(V(XOR)>1))) ? 2 : 0
B3x
DIS
DIS
((V(TIM2)<1)|((V(TI)>1.7)&(V(DIS)<1))) ? 0 : 2
B7
OUT
OUT
((((V(TIM2)<1)|(V(DOWN)>1)))|(((V(UP)<1)|(V(DIS)<1))&(V(OUT)<1))) ? 0 : 2
B13
TIM1
TIM1
(V(POR)>(0.35-0.05*V(TIM2))) ? 2 : 0
B2x
TIM2
TIM2
(V(POR)>(1.5-0.15*V(TIM2))) ? 2 : 0
Token logic
V2x
5V
R2x
22.5K
PWM
R4x
10K
TI
R1x
50K
R3x
r=((V(DIS)<1)&(V(OUT)<1) ? 10K : 100Meg)
TI
POR
C1
25p
POR
B1x
V(POR)>0 ? 1u : 0
B8
TD0
TD0
UTD
X2
TD = 10n
TD10
UTD
X1
TD = 25n
TD25
((V(OUT)>1)| ((-V(TD25)+2)<1)&(V(TD0)<1))) ? 0 : 2
B9
TO
TO
TOKOUT
TOKOUT
R7
r=(V(TIM1)>1 ? 5K : 100Meg)
((V(TIM2)>1)&((V(TD0)>1)|(V(TD10)>1))) ? 5 : 0
PWMx
R11
1K
V1x
TIM2X
V4
2
DISX
V3
Tran Generators = PULSE